LOW-NOISE, HIGH-LINEARITY ANALOG MULTIPLIER

PRIORITY CLAIM

[1] This application claims priority from European patent application No. 03425092.8, filed February 18, 2003, which is incorporated herein by reference.

TECHNICAL FIELD

[2] The present invention relates generally to the field of analog electronic circuits, and more particularly to analog multipliers, *e.g.* mixers used for Radio-Frequency (RF) telecommunications.

BACKGROUND

[3] Analog multipliers, *i.e.* circuits that takes two analog input signals and produce an output signal proportional to the product of the input signals, are frequently used in analog signal processing.

[4] In particular, analog multipliers or mixers are widely used in modern communication systems in order to realize frequency conversion or translation of modulated signals.

[5] The mixers can be classified as passive and active. Active mixers employ switching transistor pairs for current commutation, such as the so-called Gilbert cell.

[6] A typical Gilbert cell mixer comprises a differential transconductance stage, used to convert an input Radio-Frequency (RF) voltage signal (the RF modulated signal to be converted) into a differential current signal. The differential current signal is fed to two pairs of current switches or switching pairs (quad), which are cross-coupled to one another and are controlled by a voltage signal generated by a local oscillator, so as to perform a current commutation. A differential current signal generated by the two switching pairs can be fed to a load, *e.g.* a purely resistive load, so as to produce an output voltage.

[7] Active mixers are particularly attractive, and are frequently used in telecommunication applications, because they offer advantages over passive mixers, such as high conversion gain and good port-to port isolation.

[8] In particular, active mixers fabricated in MOS or CMOS technology are desirable, because they can be easily integrated in a semiconductor chip together with other analog or logic circuits.

[9] High linearity, *i.e.* low intermodulation distortion, and low noise are important features in a mixer, because they greatly affect the dynamic range of most communication systems.

[10] If properly sized, the MOSFETs used in the input stage of an active mixer demonstrate fairly good linearity. The distortion of the two switching pairs is more complex to analyze and depends both on the speed of the switching pairs and on parasitic capacitances (both linear and non linear) at the nodes where the differential current signal generated by the transconductance stage is fed to the two switching pairs (the common source nodes of the switching pairs).

[11] A problem in active mixers, especially those realized in MOS or CMOS technology, is however represented by flicker or 1/f noise. It is known that the main source of this kind of noise are the MOSFETs in the two switching pairs.

[12] In a MOS- or CMOS-technology Gilbert cell mixer, a trade-off between noise and linearity performances exists. The main limitations to high linearity and low noise come from the switching pairs. In fact, for the transconductance stage, the trade-off can be broken at the price of a higher power consumption.

[13] The flicker noise contribution of the switching stage could be reduced using low biasing currents and large area MOSFETs. Unfortunately, this would increase the parasitic capacitances and reduce the switching speed. The results would be a degraded linearity. This effect is due to the non-linear partition of the signal current between the switching MOSFETs and the parasitic capacitances at the common source nodes of the switching pairs.

[14] Thus, flicker noise reduction and increase of linearity have conflicting requirements: while low biasing currents and large MOSFETs are required to reduce the flicker noise, high biasing currents and small parasitic capacitances are required to enhance linearity.

[15] The linearity problem is worsened by the high common-mode signal at twice the frequency of the signal generated by the local oscillator present at the common source nodes of the switching pairs; such common-mode signal originates from the rectification of the large signal produced by the local oscillator. This is particularly true for switching pairs in MOS- or CMOS-technology.

[16] In D. Manstretta et al., "A 0.18μm CMOS Direct Conversion Receiver Front-END for UMTS", ISSCC 2002, Session 14, Cellular RF Wireless, Paper 14.6, a solution to overcome this effect has been suggested, consisting of a common-mode LC filter resonating at twice the frequency of the local oscillator signal. In particular, the common-mode LC filter includes two capacitors and one inductor; each capacitor has a first plate connected to the common source node of a respective switching pair, and a second plate connected to a first terminal of the inductor; the second terminal of the inductor is connected to ground.

[17] Thanks to the provision of the common-mode LC filter, the oscillation amplitude of the common source nodes of the switching pairs is greatly reduced, by virtue of the low impedance shown by the filter at twice the frequency of the local oscillator signal. The result is a considerable improvement in linearity.

[18] A drawback of this solution is that as far as the differential radio-frequency signal is concerned, the filter behaves as a capacitor connected between the common source nodes of the quad, and thus worsens the flicker noise performance of the mixer.

SUMMARY

[19] In view of the state of the art outlined above, an embodiment of the present invention improves the performance of analog multipliers, particularly Gilbert cell analog multipliers.

[20] In particular, this embodiment of the present invention provides an analog multiplier design featuring increased linearity and reduced noise.

[21] Even more in particular, ithis embodiment of the present invention achieves such increased linearity and reduced noise without significantly increasing the circuit complexity.

[22] Briefly stated, an analog multiplier according to this embodiment of the invention comprises:

[23] a first stage for converting a first analog voltage signal, for example the modulated radio-frequency signal, into a first and a second current signals;

[24] a second stage, comprising a first and a second cross-coupled current-switching pairs driven by a second voltage signal, for example generated by a local oscillator, and having respective current inputs for receiving the first and the second current signals, respectively.

[25] A compensation circuit is coupled to the current inputs of the current-switching pairs, for compensating parasitic capacitances associated with each of said current inputs of the current-switching pairs.

BRIEF DESCRIPTION OF DRAWINGS

[26] These and other features and advantages of the present invention will be made apparent by the following detailed description of some embodiments thereof, provided merely by way of non-limitative example, which will be made in connection with the attached drawings, wherein:

[27] **FIG. 1** shows a circuit diagram of an active mixer according to an embodiment of the present invention;

[28] **FIGS. 2** and **3** show equivalent circuit diagrams of the mixer of **FIG. 1** helpful for analysing the behavior thereof for differential-mode signals and common-mode signals, respectively;

[29] **FIG. 4** shows an input stage of an active mixer according to an alternative embodiment of the present invention.

DETAILED DESCRIPTION

[30] With reference to **FIG. 1**, an active mixer ***100*** according to an embodiment of the present invention is shown; in particular, the active mixer ***100*** is of the type widely used in telecommunication systems for frequency translation of the modulated signals, and includes a Gilbert cell multiplier.

[31] The mixer ***100*** conventionally comprises a first stage, or input stage ***105***, and a second stage, or output stage ***110***, connected in cascade.

[32] The input stage ***105*** is a differential transconductance stage, with a differential input receiving an input voltage signal $V_{in,RF}$; in particular, the input voltage signal $V_{in,RF}$ is a modulated radio-frequency (RF) signal, oscillating at a frequency f_{RF}.

[33] The input stage ***105*** converts the input voltage signal $V_{in,RF}$ into a first and a second current signals $I_{1,RF}$, $I_{2,RF}$. In particular, the input voltage signal $V_{in,RF}$ is applied to gate electrodes of a source-coupled pair of N-channel MOSFETs ***M1***, ***M2***, biased by a bias current generator ***115*** connected to the coupled source electrodes of the MOSFETs ***M1*** and ***M2*** and generating a bias current I_{BIAS}. The differential output of the input stage ***105*** is formed by the drain electrodes of the MOSFETs ***M1*** and ***M2***.

[34] The output stage ***110*** comprises two cross-connected source-coupled pairs of N-channel MOSFETs ***M3***, ***M4*** and ***M5***, ***M6***. A common source node ***S1*** of the source-coupled MOSFETs ***M3*** and *M4* is connected to the drain electrode of the MOSFET ***M1*** in the input stage ***105***, while a common source node ***S2*** of the source-coupled MOSFETs ***M5*** and ***M6*** is connected to the drain electrode of the MOSFET ***M2*** in the input stage ***105***.

[35] A locally generated voltage signal V_{LO} is applied to gate electrodes of the MOSFETs ***M3*** and ***M4***, and to gate electrodes of the MOSFETs ***M5*** and ***M6***. The locally-generated voltage signal V_{LO}, oscillating at a prescribed frequency f_{LO}, is typically generated by a local oscillator ***120*** connected to the gate electrodes of the MOSFETs ***M3***, ***M4***, ***M5*** and ***M6***. Cross-connection of the two source-coupled

MOSFET pairs ***M3***, ***M4*** and ***M5***, ***M6*** is achieved by connecting a drain electrode of the MOSFET ***M5*** to a drain electrode of the MOSFET ***M3***, and connecting a drain electrode of the MOSFET ***M4*** to a drain electrode of the MOSFET ***M6***.

[36] The output stage ***110*** has a differential output formed by the common drain node ***D1*** of the MOSFETs ***M3*** and ***M5***, and the common drain node ***D2*** of the MOSFETs ***M4*** and ***M6***. The output stage ***110*** provides a differential output current equal to the difference between a first output current I_{O1} (the sum of the drain currents of the MOSFETs ***M3*** and ***M5***) and a second output current I_{O2} (the sum of the drain currents of the MOSFETs ***M4*** and ***M6***).

[37] In other words, the Gilbert cell multiplier is formed by the series connection of a source-coupled MOSFET pair (the MOSFET pair ***M1*** and ***M2***) with two cross-coupled, source-coupled MOSFET pairs (the MOSFET pair ***M3*** and ***M4***, and the MOSFET pair ***M5*** and ***M6***).

[38] A load, schematized in the drawing by load elements ***LD1***, ***LD2***, is normally connected to the output of the output stage ***110***, so that the differential output current of the output stage ***110*** is converted into a differential voltage.

[39] Also schematically shown in the drawing are capacitors $C_{par,1}$ and $C_{par,2}$, connected between the common source nodes ***S1*** and ***S2***, respectively, of the source-coupled MOSFET pairs ***M3***, ***M4*** and ***M5***, ***M6*** and a reference voltage (ground) ***GND***. These capacitors $C_{par,1}$ and $C_{par,2}$ represent, in terms of lumped circuit elements, parasitic capacitances associated with the common source nodes ***S1*** and ***S2***; the main contribution to such parasitic capacitances are the capacitances associated with the PN source junctions of the MOSFETs ***M3***, ***M4***, ***M5*** and ***M6***.

[40] As mentioned in the introduction of the present description, the parasitic capacitances $C_{par,1}$ and $C_{par,2}$ affect the linearity of the mixer: high parasitic capacitance values degrade the linearity of the mixer, due to a non-linear partition of the current signal $I_{1,RF}$, $I_{2,RF}$ between the MOSFETs ***M3***, ***M4***, ***M5*** and ***M6*** and the capacitors $C_{par,1}$ and $C_{par,2}$.

[41] According to an embodiment of the present invention, an LC filter ***125*** is provided, coupled to the common source nodes ***S1*** and ***S2***. In particular, the LC filter ***125*** is a "T" filter, comprising a first and a second inductors ***L1*** and ***L2***, with a first terminal connected to the common source nodes ***S1*** and ***S2***, respectively, and a second terminal connected to a first plate of a capacitor ***C***, having a second plate connected to the ground ***GND***.

[42] As visible from the differential-mode equivalent circuit diagram of **FIG. 2**, the filter ***125*** acts as a parallel resonator for differential signals at a parallel resonance frequency f_p equal to:

$$f_p = \frac{1}{2\pi\sqrt{L \cdot C_{par}}}$$

where L is the inductance value of the two inductors ***L1***, ***L2***, and C_{par} is the capacitance value of the capacitors $C_{par,1}$ and $C_{par,2}$.

[43] As visible from the common-mode equivalent circuit diagram of **FIG. 3**, the filter ***125*** acts instead as a series resonator for common-mode signals at a series resonance frequency f_s equal to:

$$f_s = \frac{1}{2\pi\sqrt{L \cdot \frac{C}{2}}}$$

where C is the capacitance value of the capacitor ***C***.

[44] By sizing the inductance L of both the inductors ***L1*** and ***L2*** so that the parallel resonance frequency f_p is equal to f_{RF} (the frequency of the radio-frequency input signal), the parallel resonance of the filter ***125*** causes the parasitic capacitances $C_{par,1}$ and $C_{par,2}$ to be cancelled, thereby improving the mixer performance in terms of linearity. In fact, the effect of non-linear partition of the currents $I_{1,RF}$, $I_{2,RF}$ between the MOSFETs ***M3***, ***M4***, ***M5*** and ***M6*** and the capacitances $C_{par,1}$ and $C_{par,2}$ is substantially eliminated.

[45] In addition to improving the linearity of the mixer, the parallel resonance of the filter ***125*** also contributes to reducing the flicker noise. In fact, as

reported in H. Darabi and A. A. Abidi, "Noise in RF-CMOS Mixers: A simple Physical Model", IEEE Transactions on Solid State Circuits, Vol. 35, No. 1, January 2000, pages 15 to 25, the parasitic capacitances $C_{par,1}$ and $C_{par,2}$ are charged and discharged by the flicker noise of the output stage ***110*** every oscillation period of the local oscillator ***120***, and thus cause this current noise to flow to the output of the mixer. By cancelling the capacitances $C_{par,1}$ and $C_{par,2}$, the filter ***125*** substantially eliminates or strongly attenuates this contribution to the flicker noise. Moreover, the inductors ***L1*** and ***L2*** short to ground the current flicker noise coming from the differential pair that will not be up-converted because of mismatches between the MOSFETs of the two source-coupled pairs.

[46] By sizing the capacitance of the capacitor ***C*** in such a way that f_s is equal to twice the local oscillator oscillation frequency f_{LO}, the series resonance of the filter ***125*** cancels the common-mode signals at twice the frequency f_{LO} present at the common source nodes ***S1*** and ***S2***, deriving from the rectification of the large signal V_{LO} generated by the local oscillator. This improves the linearity of the mixer.

[47] In other words, by properly sizing the inductance of the inductors ***L1*** and ***L2*** and the capacitance of the capacitor ***C***, the filter ***125*** is made to behave as a short-circuit to the ground ***GND*** for common-mode signals at twice the frequency f_{LO} of the local oscillator ***120***, and as an open circuit for differential signals at the frequency f_{RF} of the radio-frequency input signal $V_{in,RF}$.

[48] It is observed that, in the practice, the two inductors ***L1*** and ***L2*** can be replaced by a single, differential inductor having overall inductance equal to twice the inductance of each of the two inductors ***L1*** and ***L2***, with a center tap for the connection to the plate of the capacitor ***C***.

[49] Thanks to the provision of the filter ***125***, the trade-off normally existing in mixers between linearity and (flicker) noise performance can be broken.

[50] The mixer according to this embodiment of the present invention is particularly adapted for front-ends of RF receivers, especially for high-frequency applications such as third-generation wireless mobile telecommunication terminals

(UMTS mobile phones) and high-frequency wireless LANs, where parasitic components are dominant.

[51] Although the present invention has been disclosed and described by way of some embodiments, it is apparent to those skilled in the art that several modifications to the described embodiments, as well as other embodiments of the present invention are possible without departing from the scope thereof.

[52] For example, **FIG. 4** shows an alternative, CMOS transconductance stage ***405***, having N-channel MOSFETs ***M11*** and ***M21*** and P-channel MOSFETs ***M21*** and ***M22*** connected in series to each other in two circuit branches, with a low-side and a high-side bias current generators ***415a*** and ***415b***.

[53] In the practice, the filter ***125*** can be realized in several ways, with a different number and a different arrangement of components.

[54] Fuirthermore, as discussed above, electronic systems such as, *e.g.*, UMT's, wireless LANs, and cell phones may include the mixer ***100***.